

Attorney Docket No.: 06666-077001 / USC 3027

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REMARKS

Reconsideration and allowance of the above-referenced application are respectfully requested.

All claims are rejected based on prior art.

The rejection alleged that one having ordinary skill in the art would make the combination of Viterbi in view of Thomson Leighton "since Thomson Leighton provides a parallel algorithm... to speed processing up". In response to this, applicants have contended and continue to contend that Viterbi et al. uses serial processing to compute his state metrics and could not be modified to use parallel processing without contradicting Viterbi's express teaching. A processor forms the metrics that serially move forward along the trellis and calculate state metrics at each step. A second processor, using the same metrics, moves backward along the trellis and serially calculates the backwards state metrics. A third processor then receives both the forward and backward state metrics to create a soft output.

In response to arguments on page 2 of the current official action, however, the patent office apparently takes issue with applicants' statement that Viterbi et al. teaches the computation of state metrics using serial prefix and suffix computations. The rejection states that these are simply the

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well-known prefix and suffix operations that Viterbi et al. chooses to use. However, it is quite clear from Viterbi et al., and specifically from column 6 lines 30-55 of Viterbi et al., that these are the specific recursions used in Viterbi et al.'s calculation. The recursions in equation 5 and 6 describe going forward and going backward to calculate the computations. The fact that there are "many other ways of doing this" does not change the fact that the teaching of Viterbi et al. must be considered as a whole. In taking this teaching as a whole, the teaching states that state metrics should be calculated using a serial computation.

Applicants will discuss in detail how the remaining prior art does not rectify these deficiencies. However, applicants would like to take issue with the statement that "there is a multitude of prior art teaching various algorithms for using the prefix and suffix computations". Prior art that is not cited in the case, has not been applied, and may not even have an appropriate date against the present application is quite plainly irrelevant to this rejection. To the extent the comment referred to the Thomson Leighton book pages, it will be discussed herein. To the effect that this refers to some hypothetical prior art, it clearly does not meet the patent office's burden of providing a *prima facie* showing of unpatentability.

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First, applicants herewith renew the contention that there is no teaching or suggestion in the Viterbi et al. art to make this specific hypothetical combination. Viterbi et al. teaches the use of serial computation. Viterbi et al. teaches that these would work perfectly well and should be used for the desired operation. In fact, the only teaching of using something other than serial computation for this purpose comes from the present application; not from Viterbi et al. and not from Thomson Leighton. The rejection states that a person having ordinary skill in the art would recognize that the serial calculation is a source of the computational intensity. Again, that recognition comes from the present application. This recognition is not supported by any of the prior art in the case. In fact, on the date of the filing of the present application, there is no evidence that anyone recognized that a serial prefix computation would be computationally excessive in any way. Therefore, the contention that a very specific portion of Viterbi et al. should be replaced by the teaching in the Thomson Leighton the article is quite clearly based in hindsight.

The Thomson Leighton excerpt is simply a mathematical textbook which refers to different kinds of arrays and trees. This includes teachings of broad concepts for use in parallel prefix and suffix operations. It says not one word about the

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specific soft input/output decoder or even that its specific teachings could be used in a soft input/output decoder. Page 1 of Thomson Leighton describes that these different techniques may provide limitations on "the network's ability to solve problems quickly". This refers to his own disclosed techniques. Therefore Thomson Leighton discloses that his techniques are calculation-limited. In view of this language why would anyone ever make the combination? Moreover, there is no teaching or suggestion that his techniques could be applied to any kind of coding, much less the specific coding defined in Viterbi et al. More specifically, there is no teaching or suggestion in either Viterbi et al. or in Thomson Leighton that a parallel prefix operation could be used in place of a serial prefix operation as described in Viterbi et al.

Page 37 of Thomson Leighton describes prefix computations. This describes how the computations can be carried out on a tree. However, the basic idea to replace serial recursions of Viterbi et al. with a parallel prefix computation is not in any way taught or suggested by the cited prior art. Even further unsuggested, moreover, is the concept of using a parallel prefix computation to perform parallel prefix and/or suffix operations to compute state metrics. With all due respect, the official action uses the teaching of the present specification to provide the teaching to the use to modify the Viterbi reference.

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Neither the primary reference nor the secondary reference teaches anything about using parallel prefix computation for state metrics. This is evident within Viterbi et al. itself. Viterbi et al. teaches a data dependency that inhibits the parallelization of components. That is, since there is a data dependency in Viterbi et al., it would be contrary to Viterbi et al.'s teaching to parallelize it at all—even assuming that there was incentive to do so. In response to arguments on page 2, the examiner takes issue with our previous statement that parallel prefix computations were not taught to compute state metrics. The rejections state that Thomson Leighton teaches the use of parallel prefix computations on page 37. At the top of page 3, the official action states that one having ordinary skill in the art "only has to recognize" that forward state metrics are prefix operations. With all due respect, this recognition, made by the Official Action, is made only with the benefit of the present specification. This is much more than simply a recognition, since it requires a complete rethinking of the way that Viterbi et al. operates.

The rejection further alleges that page 38 of Thomson Leighton teaches how to overcome data dependencies. While applicants do not believe this is true, even if true, it makes applicants' own point. Specifically, if there are data dependencies, then an operation cannot be parallelized. Viterbi

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et al. would have to contradict his express teachings in order to parallelize the operation. This is in no way taught or suggested by the cited prior art, and would require contradicting the express teaching of Viterbi et al. Specifically, Viterbi et al. teaches that it is necessary to align the data using last in first out memory elements. Consequently, in Viterbi et al., each state metric requires that the previous state metrics be previously calculated. A person having ordinary skill in the art would not be able to reconcile this with the parallel prefix operations of Thomson Leighton. In fact, because Viterbi et al.'s serial operations require dependencies from previous states, it can fairly be said that Viterbi et al. teaches away from parallelization. Any attempt to parallelize Viterbi et al. would require expressly contradicting Viterbi's express teaching.

With all due respect, therefore, the combination of these two references is in error. Moreover, even if the combination were made, a person having ordinary skill in the art would require undue experimentation to carry out parallel prefix and suffix architecture to compute the forward and backward state metrics.

Each of the claims recites either this or a very similar operation. Claim 1, for example, requires iteratively processing information using a tree structure arranged in a

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parallel prefix and suffix architecture to compute the forward and backward state metrics. As described above, this is in no way taught or suggested by the hypothetical combination of prior art. Claim 36 requires determining the soft inverse of the finite state machine "by computing forward and backward state metrics... using a tree structure arranged in a parallel prefix and suffix architecture". As described above, this is not taught or suggested by any of the references, would require hindsight for the mere combination. Even if the combination were attempted to be made, it would require contradicting the express teaching of at least one of these references. Claim 54 requires "a tree structure arranged in a parallel prefix and suffix architecture". Claim 61 includes analogous limitations as do Claims 78, 85 and 91, 93 and each of the other claims in the case. For all of these reasons, each of these claims should hence be in condition for allowance.

The dependent claims are additionally rejected based on Viterbi et al. in view of Thomson Leighton, and further in view of Benedetto. Each of these claims should be allowable by virtue of their dependency, since each of these claims include the limitations discussed above.

It is believed that all of the pending claims have been addressed in this paper. However, failure to address a specific rejection, issue or comment, does not signify agreement with or

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concession of that rejection, issue or comment. In addition, because the arguments made above are not intended to be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

Applicants ask that all claims be allowed. No fee is believed to be due, however please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,



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